Amendments to the Claims

1. (Original) In an integrated circuit chip including a plurality of metal layers and first and second supply potentials, a programmable memory cell for storing a value, the memory cell comprising:

a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias;

a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein prior to programming, said first and second metal interconnect structures are coupled at a top metal layer; and

an output coupled to one of the first and second supply potentials by at least one of said first and second metal interconnect structures, wherein a state of said output is programmable by altering at least one of the plurality of metal layers.

2. (Original) The memory cell of claim 1, further comprising multiples of said first and second metal interconnect structures coupled together to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once.

3. (Original) The memory cell of claim 2, wherein one cycle is laid out to form a ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer.

4. (Original) The memory cell of claim 3, wherein said ladder structure is arranged to form a cube-shaped structure.

5. (Original) The memory cell of claim 4, wherein the first and second supply potentials comprise two buses located in a central region of said cube-shaped structure and are accessible at each of the metal layers.

6. (Original) The memory cell of claim 5, wherein said ladder structure is arranged to form a spiral-shaped structure.

7. (Original) The memory cell of claim 6, wherein the first and second supply potentials comprise buses accessible at each of the metal layers.

8. (Original) The memory cell of claim 1, wherein each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers.

9. (Original) The memory cell of claim 1, wherein each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of a plurality of via layers.

10. (Original) In an integrated circuit chip including a plurality of metal layers and first and second supply potentials, a programmable memory cell for storing a value, the memory cell comprising:

a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias;

a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias,

an output coupled to one of the first and second supply potentials by at least one of said first and second metal interconnect structures, wherein each of said first and second metal interconnect structures can be programmed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers.

11. (Original) The memory cell of claim 10, wherein said first and second metal interconnect structures are not electrically coupled to each other at a top metal layer thereby forming two outputs for the memory cell.

12. (Original) The memory cell of claims 11, wherein one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

13. (Original) The memory cell of claim 12, wherein said first and second metal interconnect structures are arranged to form a ladder structure.

14. (Original) The memory cell of claim 12, wherein said first and second metal interconnect structures are arranged to form an offset ladder structure.

15. (Original) The memory cell of claim 12, wherein said first and second metal interconnect structures are arranged to form a stacked structure.

16. (Original) The memory cell of claim 15, wherein said stacked structure comprises first and second alternating metal interconnect patterns.

17. (Original) The memory cell of claim 16, wherein:

said first alternating metal interconnect pattern comprises first and second interspersed metal traces, and

said second alternating metal interconnect pattern comprises third and fourth interspersed metal traces, and

wherein said third and fourth interspersed metal traces form a mirror image of first and second interspersed metal traces.

18. (Original) The memory cell of claim 17, wherein said first plurality of vias interconnect ones of said first and third interspersed metal traces and said second plurality of vias interconnect ones of said second and fourth interspersed metal traces.

19. (Original) The memory cell of claim 18, wherein the memory cell is programmed at any metal layer by forming an open circuit in each of said first and second interspersed metal traces of that layer thereby splitting each metal trace into two portions, and coupling together a first portion of said first interspersed metal trace to a first portion of said second interspersed metal trace and coupling together a second portion of said first interspersed metal trace to a second portion of said second interspersed metal trace.

20. (Original) The memory cell of claim 19, wherein said open circuits and coupling is not performed in regions where vias are located.

21. (Original) The memory cell of claim 20, wherein said programming is reversible during a subsequent chip revision.

22. (Original) The memory cell of claim 19, wherein the memory cell is programmed at any of a plurality of via layers by removing two vias and inserting two vias.

23. (Currently Amended) The memory cell of claim [23] 22, wherein said programming is reversible during a subsequent chip revision.

24. (Original) The memory cell as in one of claims 21-23, wherein one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.